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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/732,240	12/07/2000	Thomas George Ference	BUR919990304US1	9501

7590 10/02/2003
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EXAMINER

CHU, CHRIS C

ART UNIT PAPER NUMBER

2815

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

09/732,240

Applicant(s)

FERENCE ET AL.

Examiner

Chris C. Chu

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--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 7, 10 - 14 and 30 - 35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 7, 10 - 14 and 30 - 35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on July 10, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1 ~ 7, 10 ~ 13 and 30 ~ 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ju et al. in view of Dalal et al.

Regarding claim 1, Ju et al. discloses in Fig. 5, Figs. 8A ~ 8C and column 5, lines 32 ~ 34 a structure comprising:

- a first substrate (12) and a second substrate (11); and
- first solder bumps (25 or 36/25) and second solder bumps (26 or 36/26) offset therebetween,

- wherein said first solder bumps and said second solder bumps are separate solder bumps disposed between said first substrate and said second substrate; and
- wherein the second solder bumps (26 or 36/26) being for aligning the first substrate and the second substrate before melting the first solder bumps.

Ju et al. does not disclose the second solder bumps having at least a portion that melts at a lower temperature than the first solder bumps. However, Dalal et al. discloses in Fig. 5 and column 8, lines 49 ~ 51 bumps (38) having at least a portion (41) that melts at a lower temperature than other bumps (20). It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the portion of Dalal et al. in the second solder bumps of Ju et al. in order to increase the yield and have a joint that has high reliability as taught by Dalal et al. in column 4, lines 53 and 54.

Regarding claims 2 and 31, Ju et al. discloses in Fig. 5 and Fig. 8C the second solder bumps (26 or 36/26) being larger than the first solder bumps.

Regarding claim 3, Ju et al. (column 5, lines 60 ~ 62) and Dalal et al. (Fig. 5 and column 8, lines 49 ~ 51) disclose the second solder bumps comprising a portion (41) having a higher concentration of tin than does the first solder bumps.

Regarding claim 4, Dalal et al. discloses in Fig. 5 and column 8, lines 49 ~ 57 the portion (41) comprising an eutectic concentration of tin.

Regarding claim 5, Dalal et al. discloses in Fig. 5 the portion (41) being adjacent to the second substrate.

Regarding claim 6, Dalal et al. discloses in Fig. 5 the portion (41) being centrally located within the second solder bump.

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Regarding claim 7, Dalal et al. discloses in Fig. 5 and column 8, lines 49 ~ 57 the portion being the entire second solder bumps.

Regarding claims 10 and 32, a further difference between Ju et al. and claimed invention is “the second solder bumps melting at a temperature at least 25 °C less than the first solder bumps.” However, Dalal et al. discloses in Fig. 5 and column 8, lines 49 ~ 57 the second solder bumps melting at a temperature at least 25 °C less than the first solder bumps. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the first and second solder bump materials of Dalal et al. as the first and second solder bump materials of Ju et al. in order to provide capable of undergoing several joining cycles as taught by Dalal et al. in column 4, lines 53 and 54.

Regarding claims 11 and 33, Ju et al. discloses in Fig. 8C the first substrate (12) comprising a first semiconductor chip.

Regarding claim 12, Ju et al. discloses in column 4, lines 22 and 23 the second substrate (11) comprising a second semiconductor chip.

Regarding claim 13, Ju et al. discloses in Fig. 8C the second chip (11) being larger than the first chip.

Regarding claim 30, Ju et al. discloses in Fig. 5, Figs. 8A ~ 8C and column 5, lines 32 ~ 34 a structure comprising:

- a first substrate (12) having a main surface with first solder bumps (25 or 36/25) and second solder bumps (26 or 36/26) separately disposed thereacross; and
- the second solder bumps being for aligning the first substrate to a second substrate before melting the first solder bumps.

Ju et al. does not disclose the second solder bumps having at least a portion that melts at a lower temperature than the first solder bumps. However, Dalal et al. discloses in Fig. 5 and column 8, lines 49 ~ 51 bumps (38) having at least a portion (41) that melts at a lower temperature than other bumps (20). It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the portion of Dalal et al. in the second solder bumps of Ju et al. in order to increase the yield and have a joint that has high reliability as taught by Dalal et al. in column 4, lines 53 and 54.

Regarding claims 34 and 35, Ju et al. discloses the second solder bumps having a uniform composition. However, Ju et al. does not disclose the second solder bumps melting at a lower temperature than the first solder bumps. Dalal et al. discloses in Fig. 5 and column 8, lines 49 ~ 57 the second solder bumps melting at a lower temperature than the first solder bumps. It would have been obvious to one of ordinary skill in the art at the time of the present invention was made to use the materials of the first and second solder bumps of Dalal et al. into the materials of the first and second solder bumps of Ju et al. in order to provide capable of undergoing several joining cycles as taught by Dalal et al. in column 4, lines 53 and 54.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ju et al. and Dalal et al. as applied to claims 1 and 11 above, and further in view of Degani et al.

Regarding claim 14, Ju et al. and Dalal et al. disclose the claimed invention except for the second chip further comprising wire bond pads for bonding to a printed circuit board. However, Degani et al. discloses in Fig. 1 the second chip (18) further comprising wire bond pads (21) for bonding to a printed circuit board (11). Thus, it would have been obvious to one of ordinary skill

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in the art at the time when the invention was made to further modify Ju et al. by using the wire bond pads as taught by Degani et al. The ordinary artisan would have been motivated to further modify Ju et al. in the manner described above for at least the purpose of increasing a bond strength between the second chip and the printed circuit board.

Response to Arguments

5. Applicant's arguments filed on July 10, 2003 have been fully considered but they are not persuasive.

On page 6, applicant argues "functionality is recited to the effect that the second solder bumps are for aligning the first substrate and the second substrate before melting the first solder bumps. A similar characterization is also present in independent claim 30. This structure and function is very different from the teachings of Ju et al. and Dalal et al., either alone or in combination." This argument is not persuasive. Ju et al. clearly shows in Figs. 8A ~ 8C the second solder bumps (26) being for aligning the first substrate (12) and the second substrate (11) before melting the first solder bumps (25).

Further, applicant argues "one skilled in the art would not read the teachings thereof as somehow suggesting that copper pad 20 is a 'solder bump'." This argument is not persuasive since this argument attempts to distinguish the claim from Ju et al. and Dalal et al. merely through semantics. Whether one refers to an element (20) as a copper deposition (column 7, line 12 in Dalal et al.) or a solder bump, there is no structural or functional difference.

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Even further, applicant argues “the ‘bumps’ comprising copper pads 20 simply do not comprise ‘solder bumps’, and applicants respectfully submit that there is no suggestion in the applied art to use Dalal et al. on only one set of solder bumps, and not the other set of solder bumps.” This argument is not persuasive. As explained in the above paragraph, since the copper pads (20) of Dalal et al. read as solder bumps, Dalal et al. has two set of solder bumps.

Finally, applicant argues “claim 10 further states that the second solder bumps melt at a temperature at least 25 °C less than the first solder bumps ... The Office action again characterizes the copper pad 20 in Dalal et al. as somehow comprising a second set of solder bumps as recited by applicant. This characterization is believed erroneous.” This argument is not persuasive. As explained in the above paragraph, since the copper pads (20) of Dalal et al. read as solder bumps. Also, as explained in the previous Office action, since the portion (41) is made of Pb (m.p. 327.4°C), Bi (m.p. 271.3°C), In (m.p. 156.2°C), Sn (m.p. 231.9°C), etc. and the material for the other bumps (20) is copper that has a melting point of 1083°C, Dalal et al. meets the claim.

For the above reasons, the rejection is maintained.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

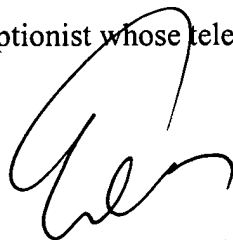
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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



EDDIE LEE

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Chris C. Chu
Examiner
Art Unit 2815

c.c.
September 29, 2003